CUSTOMER NO. 46850 ***PATENT***

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Re: Attorney Docket No. Moeller 19-8

In re application of: Lothar Benedict Erhard Josef Moeller and Chongjin Xie

Serial No.:	10/782,231	Group Art Unit:	2613
Filed:	02/19/2004	Examiner:	Kim, David S.
Matter No.:	990.0519	Phone No.:	571-272-3033

For: Method and Apparatus for Processing Optical Duobinary Signals

APPELLANTS' BRIEF (37 CFR 41.37)

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22213-1450

ATTENTION: Board of Patent Appeals and Interferences

In response to the Final Office Action dated 04/15/2008, the Advisory Action dated 07/21/2008, and further to Non-Final Office Action dated 12/23/2008, the Applicants (now Appellants) submit this Appellants' Brief in support of the appeal.

REAL PARTY IN INTEREST (37 CFR 41.37(c)(1)(i))

Other than the named inventors listed in the caption of this brief, the real party in interest is the assignee Lucent Technologies Inc. of Murray Hill, New Jersey.

RELATED APPEALS AND INTERFERENCES (37 CFR 41.37(c)(1)(ii))

None.

STATUS OF CLAIMS (37 CFR 41.37(c)(1)(iii))

Claims 1, 3, 5-9, 11, 13-20, and 22-25 are rejected. Claims 1, 3, 5-9, 11, 13-20, and 22-25 are being appealed.

STATUS OF AMENDMENTS (37 CFR 41.37(c)(1)(iv))

All previously filed amendments have been entered.

SUMMARY OF CLAIMED SUBJECT MATTER (37 CFR 41.37(c)(1)(v))

In accordance with the principles of the present invention, an optical receiver applies multiple-sampling processing to an optical signal received over a transmission link of an optical communication system. In one embodiment, the receiver has an optical-to-electrical (O/E) signal converter coupled to a decoder that processes an electrical signal generated by the O/E signal converter to generate a bit sequence corresponding to the optical signal. To generate a bit value for the bit sequence, the decoder first obtains two or more bit estimate values by sampling the electrical signal within a corresponding signaling interval two or more times. The decoder then applies a logical function to the bit estimate values, which produces the corresponding bit value for the bit sequence. (See, e.g., page 2, lines 5-13.)

The optical signal has a duty cycle greater than one (see, e.g., page 5, lines 3-5; page 10, lines 22-24; and in Figs. 4A-B). The sampling of the electrical signal includes (i) integrating the electrical signal over two different sampling windows contained within a time interval having a one-bit length to generate two respective integration results and (ii) comparing each of the two integration results with a corresponding decision threshold value to generate a corresponding bit estimate value (see, e.g., page 6, lines 3-14). An "AND" function is applied to the generated bit

estimate values to produce a bit value for the bit sequence (see, e.g., page 6, lines 14-16, and Figs. 5 and 6). The optical signal can be an optical duobinary signal (see, e.g., page 2, lines 5-7).

Independent claim 1 is directed to a method of signal processing having the steps of: converting an optical signal having a duty cycle greater than one into an electrical signal having an amplitude corresponding to optical power of the optical signal; and sampling the electrical signal using two or more sampling windows contained within a time interval having a one-bit length to generate two or more bit estimate values. The step of sampling the electrical signal has the steps of: integrating the electrical signal over a first sampling window to generate a first integration result; comparing the first integration result with a first decision threshold value to generate a first bit estimate value; integrating the electrical signal over a second sampling window to generate a second integration result; and comparing the second integration result with a second decision threshold value to generate a second bit estimate value. The method further has the step of applying a logical function to the two or more bit estimate values to generate a bit sequence corresponding to the optical signal, wherein applying the logical function comprises applying an "AND" function to the first and second bit estimate values to generate a bit of the bit sequence. Support for claim 1 can be found in Appellants' specification, e.g., in Figs. 4A-B, 5, and 6; on page 2, lines 5-13; on page 5, lines 3-5; and on page 6, lines 3-16.

Independent claim 11 is directed to an optical receiver having: a signal converter adapted to convert an optical signal having a duty cycle greater than one into an electrical signal having an amplitude corresponding to optical power of the optical signal; and a decoder coupled to the signal converter. The decoder is adapted to: (i) sample the electrical signal using two or more sampling windows contained within a time interval having a one-bit length to generate two or more bit estimate values; (ii) apply a logical function to the two or more bit estimate values to generate a bit sequence corresponding to the optical signal; (iii) integrate the electrical signal over a first sampling window to generate a first integration result; (iv) compare the first integration result with a first decision threshold value to generate a first bit estimate value; (v) integrate the electrical signal over a second sampling window to generate a second integration result; and (vi) compare the second integration result with a second decision threshold value to generate a second bit estimate value. The decoder comprises an "AND" gate adapted to apply an "AND" function to the first and second bit estimate values to generate a bit of the bit sequence. Support for claim 11 can be found in

Appellants' specification, e.g., in Figs. 4A-B, 5, and 6; on page 2, lines 5-13; on page 5, lines 3-5; and on page 6, lines 3-16.

Independent claim 20 is directed to an optical communication system having an optical receiver coupled to an optical transmitter via a transmission link. The optical receiver comprises: a signal converter adapted to convert an optical signal having a duty cycle greater than one into an electrical signal having an amplitude corresponding to optical power of the optical signal; and a decoder coupled to the signal converter. The decoder is adapted to: (i) sample the electrical signal using two or more sampling windows contained within a time interval having a one-bit length to generate two or more bit estimate values; (ii) apply a logical function to the two or more bit estimate values to generate a bit sequence corresponding to the optical signal; (iii) integrate the electrical signal over a first sampling window to generate a first integration result; (iv) compare the first integration result with a first decision threshold value to generate a first bit estimate value; (v) integrate the electrical signal over a second sampling window to generate a second integration result; and (vi) compare the second integration result with a second decision threshold value to generate a second bit estimate value. The decoder comprises an "AND" gate adapted to apply an "AND" function to the first and second bit estimate values to generate a bit of the bit sequence. Support for claim 20 can be found in Appellants' specification, e.g., in Figs. 1, 4A-B, 5, and 6; on page 2, lines 5-13; on page 3, lines 23-31; on page 5, lines 3-5; and on page 6, lines 3-16.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL (37 CFR 41.37(c)(1)(vi))

A first issue is whether claims 1, 3, 5, 7-9, 11, 14-20, and 23-25 are unpatentable under 35 U.S.C. 103(a) over Moeller (US2003/0170022, hereafter Moeller-022), with reference to Singh (the NPL document entitled "Modulating Pulses in Long-Haul Optics Systems," article ID 16504367 from http://www.commsdesign.com), in view of Applicant's admitted prior art (AAPA), further in view of Engl (U.S. Patent No. 7,173,993), and further in view of concession by Applicant (CA).

A second issue is whether claims 6, 13, and 22 are unpatentable under 35 U.S.C. § 103(a) over Moeller-022, with reference to Singh, in view of Applicant's admitted prior art (AAPA), further in view of Engl (U.S. Patent No. 7,173,993), further in view of concession by Applicant (CA), and further in view of Yonenaga (the NPL document entitled "Dispersion-Tolerant Optical Transmission System Using Duobinary Transmitter and Binary Receiver," Journal of Lightwave Technology, 1997, v. 15, pages 1530-1537).

Moeller-022, Singh, Engl, and Yonenaga are referred to herein collectively as "the cited references." The AAPA and CA are referred to herein collectively as "the cited teachings."

ARGUMENT (37 CFR 41.37(c)(1)(vii))

Rejections of claims 1, 3, 5, 7-9, 11, 14-20, and 23-25 under 35 U.S.C. § 103(a) over Moeller-022, with reference to Singh, in view of Applicant's admitted prior art (AAPA), further in view of Engl, and further in view of concession by Applicant (CA)

The method defined in claim 1 has the steps of: (i) **integrating** the electrical signal **over a** first sampling **window** to generate a first integration result; (ii) comparing the first **integration** result with a first decision threshold value to generate a first bit estimate value; (iii) **integrating** the electrical signal **over a** second sampling **window** to generate a second integration result; (iv) comparing the second **integration** result with a second decision threshold value to generate a second bit estimate value; and (v) applying an **"AND" function** to the first and second bit estimate values to generate a bit of the bit sequence. Claim 1 further recites the limitation of **a duty cycle greater than one**.

Steps of Integrating and Comparing

In the rejection of claim 1, in the final office action dated 04/15/2008, the Examiner cited and relied on Fig. 4 of Moeller-022 as teaching the "integrating" steps recited in claim 1. In particular, the Examiner stated that "integration for the left [and right] sampling point is implied in the decision circuit 240." (See page 2 of the final office action dated 04/15/2008.)

In the subsequent rejection of claim 1, on page 4 of the non-final office action dated 12/23/2008, the Examiner effectively retracts the previous rejection and admits that Moeller-022 "does not expressly disclose" the "integrating" steps recited in claim 1. Since the previous rejection relied on Moeller-022, with reference to Singh, the Appellants submit that this Examiner's admission is also an implicit admission of non-obviousness of the "integrating" steps recited in claim 1 over Moeller-022, with reference to Singh.

To remedy the admitted deficiencies of Moeller-022, with reference to Singh, the Examiner cites and relies on (i) Engl's Figs. 3, 4, and 6 (pointing to sampling instants T2, T21, and T22) and (ii) the AAPA (the paragraph beginning at page 4, line 33, of Appellants' own specification). For the following reasons, the Appellants submit that Examiner's reliance on the cited portions of Engl and AAPA is misguided and improper.

Referring first to Engl, the Appellants note that the Examiner attempts to use Engl's **sampling instants** T2, T21, and T22 to establish that the use of multiple **sampling windows** (as contrasted with **sampling points** of Moeller-022) within a single bit period was known in the relevant prior art.

In response, the Appellants submit that a sampling instant of Engl is in fact a sampling point and is **not** an example of a sampling window recited in claim 1.

First of all, the Appellants direct Board's attention to the fact that "an instant" is commonly understood to be "an infinitesimal space of time; *esp*: a **point** in time separating two states" (emphasis added; see Merriam-Webster's Collegiate Dictionary, Eleventh Edition, Merriam-Webster, Inc., Springfield, Massachusetts, 2003, p. 648). Since Engl does not contain an explicit definition of the term "instant" to override the commonly accepted plain meaning of this word, it is submitted that Engl's term "instant" should be construed according to its plain meaning, i.e., a point in time.

Second, the Appellants direct Board's attention to the fact that the Examiner refers to "the finite widths of sampling instants T2, T21, and T22" (see page 4 of the office action dated 12/23/2008). However, the Examiner fails to provide a pointer to an exact place in Engl that unambiguously states that sampling instants T2, T21, and T22 have finite widths. It appears that the examiner confuses the concepts of "sampling pulses" (see, e.g., Engl's col. 2, lines 65-67) and "sampling instants" used by Engl. While it is true that Engl's "sampling pulses" have finite widths, e.g., as indicated in Engl's Fig. 6, it is also true that this fact alone cannot and does not lead to the conclusion that a "sampling instant" of Engl is an example of a "sampling window" recited in claim 1, notwithstanding Examiner's assertions to the contrary.

As known in the art, the term "sampling" refers to a process of converting a continuous signal into discrete data. The term "point sampling" designates a process of obtaining a value of the continuous signal at a particular fixed instant (i.e., point) in time. Although technical limitations of a real-life electronic circuit usually cause it to have a finite time resolution, an electronic circuit adapted for "point sampling" is normally designed to generate signal samples that approximate the ideal point samples as closely as practically possible. The latter means that the characteristics of the electronic circuit are chosen so that the signal does not significantly change while a sample of the signal is being generated by the electronic circuit. It is submitted that the "finite widths" of Engl's "sampling pulses" are in fact selected to implement point sampling, and **not** window sampling, as

the Examiner contends. The fact that Engl repeatedly and consistently uses the term "sampling instant" while describing its sampling technique further supports this conclusion.

In contrast, an electronic circuit adapted for window sampling and signal integration is designed to generate a signal sample that represents an integral of the signal over a time interval, and not just a point sample of the signal. A typical purpose of integrating a signal is to obtain its average value over the sampling-window duration or to smooth out undesirable (e.g., noise-induced) signal fluctuations. This means that the duration of the sampling window is normally chosen so that the signal is able to change or fluctuate significantly within the sampling window. Clearly, **sampling** a signal **at a point or instant** and **integrating** a signal **over a** sampling **window** are two **very different** signal processing techniques because the former aims at obtaining a snap-shot of the signal while the latter allows the signal to evolve while being measured. It is therefore submitted that the Examiner's contention that signal integration can be implied from point or instant sampling of the signal is unfounded and improper.

In Appellants' opinion, a sensible test for what is a sampling "point" and what is a sampling "window" has to be based on a meaningful **functional distinction** between these two entities within the framework of a particular physical application. It is submitted that one workable functional distinction between a sampling "point" and a sampling "window" can be articulated by looking at what different sampling circuits do with their respective signals during the corresponding finite sampling times. For example, a sampling circuit designed to use a sampling "point" substantially obtains a snap-shot of the signal. This functionality is accomplished through the use of a relatively short sampling time, during which the signal is **not** able to change significantly. In contrast, a sampling circuit designed to use a sampling "window" obtains a signal measure that takes into account an inherent variability of the signal within the sampling "window." This functionality is accomplished through the use of a relatively long sampling time, during which the signal can change or fluctuate significantly. Note that, with this approach, the frequency spectrum of the signal itself provides a time scale based on which a well-defined demarcation line can be drawn between sampling "points" and sampling "windows."

Turning now to Engl, one finds that: (i) there is no teaching or suggestion that a significant signal change or variation occurs while the signal is being sampled at a sampling instant and (ii) no significant signal change or variation can be discerned within the widths of the sampling pulses graphically shown in Engl's Figs. 3, 4, and 6. The Appellants submit that a reasonable inference

from these observations is that the sampling method disclosed in Engl obtains and relies on snap-shots of the signal.

In contrast, Appellants' specification devotes a great deal of text and effort to explain that significant signal fluctuations and/or variability can occur within a sampling window. For example, page 4, lines 34-36, describe "noise averaging" effected by the "relatively large width" of the "sampling window." Signal traces shown in Appellants' Fig. 3A graphically indicate that, even in the absence of noise, there can be significant signal variability within a sampling window. The paragraph starting at page 5, line 6, discusses the contribution of noise and of the leading and trailing edges into the integration results.

Based on these analyses and the articulated distinction between a sampling "point" or "instant" and a sampling "window," it is clear that Engl does not explicitly teach or implicitly suggest a sampling step that uses sampling "windows," notwithstanding the Examiner's assertions to the contrary.

Referring now to the alleged AAPA (Appellants' paragraph beginning at page 4, line 33), the Appellants note that the Examiner attempts to use the cited text to establish that "the 'integrating...over a...sampling window' and 'integration' limitations were known in the relevant prior art.

In response, the Appellants submit that (i) Examiner's interpretation of that paragraph is over-broad and (ii) the paragraph's contents do not provide a substantive basis for the rejection of the limitations in question.

Appellants' paragraph in question (beginning at page 4, line 33) reads as follows:

> In a typical prior-art configuration, the sampling window has a relatively large width, e.g., greater than 30% of the bit length. One consideration for choosing a relatively large width value is that longer integration times typically provide noise averaging, which can reduce decoding errors. It is generally believed that setting a relatively narrow sampling window will reduce the benefits of noise averaging and detrimentally affect performance of receiver **200**. However, for signals affected by dispersion, using a relatively wide sampling window increases decoding errors, e.g., due to wrong interpretation of zeros in "101" binary fragments. For similar reasons,

analogous decoding errors may be caused by dispersion-free signals utilizing relatively large duty-cycle values, e.g., greater than 1 (see Fig. 3A).

First of all, the Appellants note that this paragraph appears in the "DETAILED DESCRIPTION" section of Appellants' specification. As such, the paragraph, as a whole, cannot be automatically assumed to be admitted prior art. Certainly, the third and last sentences of the paragraph are **not** admitted prior art because they refer to Appellants' Fig. 2 (in which receiver **200** is shown) and Fig. 3A, respectively, none of which is labeled as prior art. Only the first sentence of the paragraph explicitly mentions "prior art." Yet, in the rejection of claim 1, on page 4 of the office action dated 12/23/2008, the Examiner treats the **whole** paragraph as AAPA. The Appellants submit that this treatment is obviously improper. The Appellants further submit that the AAPA portion of the paragraph in question is in fact limited to the first sentence **only** because only that sentence and that sentence alone contains an explicit reference to the "prior art."

If one now examines the first sentence of the above-quoted paragraph, one will find that, at most, it admits that a typical prior-art configuration uses a sampling window having a width greater than 30% of the bit length. Thus, when properly discerned, the AAPA of the above-quoted paragraph does not talk about "integrating" and/or "integration" and, as such, cannot possibly support the rejection of the corresponding limitations of claim 1, notwithstanding the Examiner's assertions to the contrary.

In addition, the Appellants direct Board's attention to the fact that claim 1 contains, not one, but **four** limitations that recite either "integrating" or "integration." Even if the second sentence of the above-quoted paragraph were to be interpreted as admitted prior art (with respect to which the Appellants submit that it can **not** and should **not**), then the first two sentences, taken together, would **not**, nevertheless, support the rejection of **all four** relevant limitations. For example, the first two sentences certainly do not disclose an example of two different integration steps using two different sampling windows located within a single bit period, as required by claim 1.

For all these reasons, it is submitted that the Examiner's contention that the relied upon references and teachings explicitly teach or implicitly suggest the "integrating"/"integration" limitations of claim 1 is unfounded and improper. It is therefore submitted that the relied upon references and teachings do not provide an adequate basis for, and therefore cannot support, the conclusion of obviousness with respect to these limitations of claim 1.

Duty Cycle Greater Than One

In the rejection of claim 1, on page 3 of the office action dated <u>12/23/2008</u>, the Examiner finds the limitation of "a duty cycle greater than one" to be obvious over the combination of Moeller-022 and Singh. More specifically, the Examiner states that claim 9 in Moeller-022 recites non-return-to-zero (NRZ) pulses. The Examiner further states that Singh discloses NRZ pulses that are "on for an entire period," which corresponds to a duty cycle of one, and that Singh further discloses pulse broadening due to dispersion in the optical fiber, which is capable of increasing the duty cycle to greater than one. The Examiner then concludes that, based on Singh, "one would expect NRZ pulses received by Moeller to [possibly] have a duty cycle greater than one." (See also page 2 of the final office action dated <u>04/15/2008</u>.)

While it is true that Singh discloses NRZ pulses that are "on for an entire period" and that those pulses can be broadened by dispersion in the optical fiber, the Appellants submit that these teachings alone are not sufficient to render the above-specified limitation of claim 1 obvious over the combination of Moeller-022 and Singh. Rather, the conclusion of obviousness hinges on the question of whether it would have been obvious to one of ordinary skill in the art to apply the method disclosed in Moeller-022 to an NRZ signal having a duty cycle greater than one. For the following reasons, the Appellants submit that it would not have been obvious to one of ordinary skill in the art to apply the method disclosed in Moeller-022 to an NRZ signal having a duty cycle greater than one, notwithstanding the Examiner's assertions to the contrary.

First of all, the Appellants note that the exact language of Moeller-022's claim 9 is as follows: "The method of claim 8, wherein said input optical signal is a non-return-to-zero (NRZ) optical pulse." Thus, it is clear that Moeller-022's claim 9 only specifies the type of the optical signal (which is NRZ) but does not specify its duty cycle. In fact, inspection of the entire specification in Moeller-022 reveals that the term "duty cycle" is not mentioned there at all. The only examples in Moeller-022 from which the duty cycle can be inferred are shown in Figs. 1, 3, and 4. More specifically, the example shown in Fig. 1 has a label "10 Gb/s 33% RZ TX," the most reasonable interpretation of which is that it refers to a return-to-zero (RZ) signal having a duty cycle of 33% (or 0.33). The duty cycle for the examples shown in Figs. 3 and 4 can be estimated as a ratio of the pulse width to the bit-slot width. That ratio and therefore the duty cycle does not exceed 50% (or 0.5) by any measure. Thus, Moeller-022 does not explicitly teach or implicitly suggest that its method can be applied to process an optical signal having a duty cycle greater than one.

Second, the Appellants note that, by definition, an NRZ signal is a signal that does not fall to a zero level between two adjacent "ones." The NRZ signal does fall to the zero level when the bit sequence that it represents has a binary "zero." The Appellants further note that the NRZ designation alone does not say anything about the duty cycle of the signal. Furthermore, it is clear that the concept of "duty cycle" does not apply to a continuous sequence of NRZ "ones" because it is practically impossible to tell where the preceding "one" ends and the next "one" begins. However, the duty cycle of an NRZ signal can still be inferred from the position of the transition edge between a "zero" and an adjacent "one." In particular, in an optical NRZ signal having a duty cycle greater than one, the transition edge between an optical "zero" and an adjacent optical "one" is located inside the bit interval corresponding to the "zero."

Finally, the Appellants note that the method of Moeller-022 is aimed at reducing the number of jitter-induced decoding errors (see, e.g., Moeller-022's paragraphs [0002] and [0007] and claims 1 and 14). For an NRZ signal having a duty cycle greater than one, the effect of jitter is to randomly change the position of the transition edge between an optical "zero" and an optical "one" within the bit interval corresponding to the optical "zero." This random position variation creates a probability for at least one of the two sampling "points" inside the "zero" bit interval to overlap with the transition edge and cause decision circuit **240** to output a "one," instead of a "zero," as a corresponding sample of the signal. An "OR" function applied to a bit combination having at least one "one" returns a "one," which represents a decoding error for the optical "zero." Thus, if applied to an optical NRZ signal having a duty cycle greater than one, the method of Moeller-022 would increase, rather than decrease, the number of jitter-induced decoding errors due to the additional decoding errors in the "zero" bit intervals. Since the aim of the method of Moeller-022 is exactly the opposite of this result, the Appellants submit that one of ordinary skill in the art would not be motivated to apply the method of Moeller-022 to NRZ signals having a duty cycle greater than one.

On page 5 of the advisory action dated <u>07/21/2008</u>, the Examiner attempts to counter these arguments by stating that:

> Moeller-022 ***already*** positively teaches the use of an NRZ signal (Moeller-022, claim 9). Singh ... shows that pulses generally undergo broadening in optical fiber... Accordingly, ***without*** any consideration of obviousness, one would expect the NRZ signal of Moeller-022 to experience pulse broadening, which would result in a duty cycle greater than one.

In response, the Appellants submit that the Examiner cannot possibly make an obviousness-type rejection and, at the same time, take "any consideration of obviousness" out of the picture. If the Examiner wanted to make a rejection "***without*** any consideration of obviousness," then he should have made a rejection under 35 U.S.C. § 102, and not under 35 U.S.C. § 103(a), which, of course, he could not properly do. It appears that, with respect to the "duty cycle" limitation, the Examiner conveniently chose to disregard the familiar framework set forth in Graham v. John Deere Co. and subsequently clarified in KSR International Co. v. Teleflex Inc. The Appellants submit that, due to the evident deviation from the proper examination guidelines, the part of the rejection directed at the "duty cycle" limitation must fall for want of proper methodology.

On page 15 of the office action dated 12/23/2008, the Examiner attempts to counter these arguments by referring to MPEP 2131.01.

In response, the Appellants note that MPEP 2131.01 addresses rejections under 35 U.S.C. § 102 only (see, e.g., the title of MPEP 2131.01: "2131.01 Multiple Reference **35 U.S.C. 102** Rejections," emphasis added). However, the present rejection of claim 1 is made under 35 U.S.C. § 103. Therefore, for the rejection to be proper, the Examiner **must** follow the framework of Graham v. John Deere Co. and KSR International Co. v. Teleflex Inc., which the Examiner **failed** to do. In particular, the Examiner failed to establish that it would have been obvious to one of ordinary skill in the art to apply the method disclosed in Moeller-022 to signals having "a duty cycle greater than one."

The Appellants submit that the above presented substantive arguments on this point show that, in fact, it would **not** have been obvious to one of ordinary skill in the art to apply the method disclosed in Moeller-022 to signals having "a duty cycle greater than one" because the resulting method would increase the number of jitter-induced decoding errors. However, in the office action dated 12/23/2008, the Examiner did not even attempt to address or refute these substantive arguments. Instead, the Examiner chose to improperly take the "duty cycle" limitation out of the context of the claim and simply state that this limitation is inherent to the teachings of Moeller-022. Clearly, this approach is improper and cannot possibly support the conclusion of obviousness with respect to the limitation in question.

For all these reasons, the Appellants submit that the Examiner's conclusion that the "duty cycle" limitation of claim 1 is obvious over the cited references and teachings is unsubstantiated and improper.

Step of Applying an AND Function

In the rejection of claim 1, on pages 4-5 of the office action dated 12/23/2008, the Examiner admits that Moeller-022 "does not expressly disclose" the step of "applying an 'AND' function." However, on page 5, the Examiner asserts that:

> Rather, Moeller discloses the application of an "OR" function (e.g., gate 260 in Fig. 2, gate 570 in Fig. 5) [and] the option of applying other alternative circuitry (paragraph [0020]). The usage of the "OR" function is to reduce the error probability for logical "1" values (paragraph [0027]). Logically speaking, an "AND" function is an "OR" function for "0" values. That is, a regular "OR" function outputs a "1" if any input is "1". Similar in operation, a regular "AND" function outputs a "0" if any input is a "0". At the time the invention was made, it would have been obvious to one of ordinary skill in the art to notice that such similar operation is an obvious variation of the method of Moeller. One of ordinary skill in the art would have been motivated to employ an "AND" function for the similar reason of employing an "OR" function, i.e., to reduce the probability of a particular bit estimate value, e.g., "0" values.

First, the Appellants submit that, as correctly noticed by the Examiner in the above-cited passage, changing the application of an "OR" function to the application of an "AND" function requires a recognition of the fact that incorrect decoding of optical "zeros," rather than optical "ones," can be a major source of decoding errors. However, that **recognition is absent** in Moeller-022 because Moeller-022 primarily deals with decoding of optical return-to-zero (RZ) signals having a relatively small duty cycle, e.g., about 33% (see, e.g., Moeller-022's Figs. 3-4 and paragraphs [0018]-[0019]). When an optical signal has a small duty cycle, transmission impediments, such as jitter, do not increase the error probability for optical "zeros" (see, e.g., the last sentence of Moeller-022's paragraph [0026]). Therefore, there is no problem of incorrect decoding of optical "zeros" in Moeller-022, and this problem is not recognized there. In contrast, the present application recognizes that, for optical signals broadened by dispersion and/or having a relatively large duty cycle, e.g., about 100%, incorrect decoding of optical "zeros" can be a major source of decoding errors (see, e.g., Appellants' Figs. 3A and 4A-B and page 5, lines 1-5).

Second, the Appellants submit that Moeller-022 does not expressly suggest applying logic functions other than the "OR" function, notwithstanding the Examiner's statement to the contrary.

More specifically, the relevant portion of the relied-upon paragraph [0020] in Moeller-022 reads as follows:

> Although the front-end pre-amplified receiver **200** of FIG. 2 is depicted as a relatively complex receiver, a less complex conventional front-end pre-amplified receiver can also be implemented within various embodiments of the present invention. Additionally, **although** the logic circuitry **260** of FIG. 2 is **depicted as an OR logic gate, other circuitry** or devices that are **able to determine a resulting logic state** of at least one input signal **can be implemented** with the concepts of the present invention. [Emphasis added.]

It is clear from the context of paragraph [0020] that what is being discussed here is **different hardware implementations of the same logic functionality**, and **not a different logic functionality** as implied by the Examiner. Indeed, the first of the above-cited sentences talks about replacing relatively complex front-end pre-amplified receiver **200** by a less complex receiver capable of performing the same function as receiver **200**. Likewise, the second of the above-cited sentences talks about **replacing an OR logic gate with a different circuit capable of performing the same logic function as the OR gate**. The Appellants submit that reading a suggestion of a logic function change into the above-cited text is unwarranted.

Finally, and perhaps most importantly, changing the "OR" functionality of logic circuitry **260** to a different logic functionality, e.g., the "AND" functionality, would increase, rather than decrease, the number of decoding errors in receivers disclosed in Moeller-022 (see, e.g., Moeller-022's Fig. 4). More specifically, the two signal samples shown in Moeller-022's Fig. 4 will cause decision circuit **240** to output a "zero" for the left sample and a "one" for the right sample. An "AND" function applied to a "zero-one" combination returns a "zero." The latter represents a decoding error for the signal shown in Moeller-022's Fig. 4. The Appellants submit that a modification or variant that would actually worsen the performance of the device cannot be properly read into the device description or assumed obvious to one of ordinary skill in the art.

To summarize, Moeller-022 (1) does **not** recognize that incorrect decoding of optical "zeros," rather than optical "ones," can be a major source of decoding errors and (2) does **not** suggest an application of a logical function other than the "OR" function for the purpose of correcting jitter-induced decoding errors. The Appellants submit that, in the absence of such recognition or suggestion, it would not have been obvious to one of ordinary skill in the art to

change an "OR" function in Moeller-022 to an "AND" function recited in claim 1, notwithstanding the Examiner's assertion to the contrary.

On page 5 of the office action dated 12/23/2008, the Examiner further states that "it is an extremely common and obvious practice to consider inverse scenarios" and that "Applicant appears to express the same opinion of obviousness of different scenarios in [concession by Applicant] CA...(Applicant's specification, p. 6, l. 17-30)." In particular, the Examiner cites and relies on the following sentence in Appellants' specification: "One skilled in the art will appreciate that, depending on the type of impediment and/or waveform shape, other logical functions or other numbers (e.g., three or more) of sampling windows may similarly be employed."

In response, the Appellants note that the above-quoted sentence is preceded by a discussion of the use of "AND" and "OR" functions given in reference to Appellants' Fig. 3A, and **not** in reference to Moeller-022. Thus, if anything, the relied-upon sentence implies that one of ordinary skill in the art would be able to use different combinations of logic functions in view of Appellants' specification, and **not in view of Moeller-022**. However, the Examiner erroneously uses the alleged concession by Applicant (CA) is if it were made in reference to Moeller-022, which it is **absolutely not**. It is therefore submitted that Examiner's reliance on the alleged concession by Applicant (CA) is in error and has no justification. Since the Examiner explicitly relies on the alleged CA in the rejection of claim 1, it follows that the obviously erroneous nature of this reliance renders the rejection of claim 1 over the CA substantively deficient and incomplete.

For all these reasons, the Appellants submit that the Examiner's conclusion that the "AND function" limitation of claim 1 is obvious over the cited references and teachings is unsubstantiated and improper.

Combination of Features

Even if each of the three above-discussed limitations of claim 1 were obvious over the cited references and teachings, which the Appellants do **not** admit, the Appellants submit that the combination of the corresponding features would still be non-obvious.

In particular, the Appellants would like to point out that the three above-discussed features have a positive synergistic effect on the performance of the optical receiver. For example, the steps of integrating help to smooth out the optical spikes produced by photon bursts generated by spontaneous beat noise and/or thermal noise (see, e.g., Appellants' Fig. 3B). The step of applying the logical "AND" function then further guards against a decoding error when such an optical spike

is so large as to still cause one of the smoothed-out samples in a "zero" bit interval to overshoot the decision threshold. As already indicated above, integrating the signal and applying the "AND" function to the signal samples is particularly beneficial for signals having a duty cycle greater than one because decoding errors for such signals are dominated by the errors in the "zero" bit intervals. Thus, claim 1 defines a robust signal processing scheme that is significantly more advantageous than a processing scheme utilizing each of the above-discussed features separately, rather than all three of them together as required by claim 1 (see, e.g., Appellants, Figs. 7 and 8A-B and the corresponding description).

For all these reasons, the Appellants submit that claim 1 is non-obvious over the cited art and that the rejection of claim 1 should be withdrawn. For similar reasons, it is submitted that claims 11 and 20 are allowable over the cited references. Since claims 3, 5-9, 13-19, and 22-25 depend variously from claims 1, 11, and 20, it is further submitted that those claims are allowable over the cited references. The Appellant submits therefore that the rejections of claims 1, 3, 5-9, 11, 13-20, and 23-25 under § 103 have been overcome.

<u>Rejections of claims 6, 13, and 22 under 35 U.S.C. § 103(a) over Moeller-022, with reference to Singh, in view of Applicant's admitted prior art (AAPA), further in view of Engl, further in view of concession by Applicant (CA), and further in view of Yonenaga</u>

Claims 6, 13, and 22 depend from claims 1, 11, and 20, respectively.

The Appellants submit that the rejection of claim 6 should be withdrawn at least for the reasons explained above in reference to the rejection of claim 1 and because (i) Yonenaga does not remedy the above-indicated deficiencies of other cited references and teachings with respect to claim 1 and (ii) the improper rejection of claim 1 renders the rejection of claim 6 substantively incomplete and improper.

The Appellants further submit that the rejection of claim 13 should be withdrawn at least for the reasons explained above in reference to the rejection of claim 13 and because (i) Yonenaga does not remedy the above-indicated deficiencies of other cited references and teachings with respect to claim 11 and (ii) the improper rejection of claim 11 renders the rejection of claim 13 substantively incomplete and improper.

The Appellants further submit that the rejection of claim 22 should be withdrawn at least for the reasons explained above in reference to the rejection of claim 20 and because (i) Yonenaga does

not remedy the above-indicated deficiencies of other cited references and teachings with respect to claim 20 and (ii) the improper rejection of claim 20 renders the rejection of claim 6 substantively incomplete and improper.

CLAIMS APPENDIX (37 CFR 41.37(c)(1)(viii))

1. (Previously presented) A method of signal processing, comprising:

converting an optical signal having a duty cycle greater than one into an electrical signal having an amplitude corresponding to optical power of the optical signal;

sampling the electrical signal using two or more sampling windows contained within a time interval having a one-bit length to generate two or more bit estimate values, wherein sampling the electrical signal comprises:

integrating the electrical signal over a first sampling window to generate a first integration result;

comparing the first integration result with a first decision threshold value to generate a first bit estimate value;

integrating the electrical signal over a second sampling window to generate a second integration result; and

comparing the second integration result with a second decision threshold value to generate a second bit estimate value; and

applying a logical function to the two or more bit estimate values to generate a bit sequence corresponding to the optical signal, wherein applying the logical function comprises applying an "AND" function to the first and second bit estimate values to generate a bit of the bit sequence.

2. (Canceled)

3. (Original) The method of claim 1, wherein:

each sampling window has a width;

the electrical signal has a series of waveforms comprising first and second pluralities of waveforms, wherein each waveform of the first plurality represents a binary "0" and each waveform of the second plurality represents a binary "1"; and

for each sampling window:

a waveform is integrated over the sampling window width to generate a corresponding bit estimate value; and

the sampling window width is selected to reduce contribution of the second plurality of waveforms into integration results corresponding to the first plurality of waveforms.

4. (Canceled)

5. (Previously presented) The method of claim 1, wherein the first decision threshold value is different from the second decision threshold value.

6. (Original) The method of claim 1, wherein the optical signal is an optical duobinary signal.

7. (Previously presented) The method of claim 1, comprising:

generating a first clock signal based on the electrical signal;

multiplying a frequency of the first clock signal to generate a second clock signal; and

sampling the electrical signal at a sampling rate corresponding to the second clock signal to generate a bit stream carrying the first and second bit estimate values.

8. (Previously presented) The method of claim 7, comprising:

separating the first and second bit estimate values from the bit stream while discarding all other bits of the bit stream.

9. (Previously presented) The method of claim 1, comprising:

generating a clock signal based on the electrical signal;

sampling first and second copies of the electrical signal at a sampling rate corresponding to the clock signal, wherein:

the first copy is sampled to generate the first bit estimate value;

the second copy is sampled to generate the second bit estimate value; and

the first and second copies are sampled with a relative time delay.

10. (Canceled)

11. (Previously presented) An optical receiver, comprising:

a signal converter adapted to convert an optical signal having a duty cycle greater than one into an electrical signal having an amplitude corresponding to optical power of the optical signal; and

a decoder coupled to the signal converter and adapted to:

(i) sample the electrical signal using two or more sampling windows contained within a time interval having a one-bit length to generate two or more bit estimate values;

(ii) apply a logical function to the two or more bit estimate values to generate a bit sequence corresponding to the optical signal;

(iii) integrate the electrical signal over a first sampling window to generate a first integration result;

(iv) compare the first integration result with a first decision threshold value to generate a first bit estimate value;

(v) integrate the electrical signal over a second sampling window to generate a second integration result; and

(vi) compare the second integration result with a second decision threshold value to generate a second bit estimate value, wherein:

the decoder comprises an "AND" gate adapted to apply an "AND" function to the first and second bit estimate values to generate a bit of the bit sequence.

12. (Canceled)

13. (Original) The receiver of claim 11, wherein the optical signal is an optical duobinary signal.

14. (Previously presented) The receiver of claim 11, comprising:

a decision circuit coupled to the signal converter;

a clock recovery circuit coupled to the signal converter and adapted to generate a first clock signal based on the electrical signal; and

a clock multiplier coupled between the clock recovery circuit and the decision circuit and adapted to multiply a frequency of the first clock signal to generate a second clock signal, wherein the decision circuit is adapted to sample the electrical signal at a sampling rate corresponding to the second clock signal to generate a bit stream carrying the first and second bit estimate values.

15. (Previously presented) The receiver of claim 14, comprising:

a de-multiplexer having an input port and a plurality of output ports, wherein:

the input port is coupled to the decision circuit;

a first output port is adapted to receive a signal corresponding to the first bit estimate value; and

a second output port is adapted to receive a signal corresponding to the second bit estimate value, wherein the "AND" gate is coupled to the first and second output ports.

16. (Previously presented) The receiver of claim 11, comprising:

first and second decision circuits, each coupled to the signal converter; and

a clock recovery circuit coupled between the signal converter and the first and second decision circuits and adapted to generate a clock signal based on the electrical signal, wherein:

each decision circuit is adapted to sample the electrical signal at a sampling rate corresponding to the clock signal;

the first decision circuit is adapted to generate the first bit estimate value;

the second decision circuit is adapted to generate the second bit estimate value; and

the first and second decision circuits sample the electrical signal with a relative time delay.

17. (Previously presented) The receiver of claim 16, wherein the "AND" gate is coupled to the first and second decision circuits.

18. (Previously presented) The receiver of claim 16, wherein each decision circuit is adapted to:

integrate the electrical signal over a respective sampling window to generate a respective integration result; and

compare the respective integration result with a respective decision threshold value to generate a bit estimate value.

19. (Original) The receiver of claim 18, wherein the first and second decision circuits use different decision threshold values.

20. (Previously presented) An optical communication system, comprising an optical receiver coupled to an optical transmitter via a transmission link, wherein the optical receiver comprises:

a signal converter adapted to convert an optical signal having a duty cycle greater than one into an electrical signal having an amplitude corresponding to optical power of the optical signal; and

a decoder coupled to the signal converter and adapted to:

(i) sample the electrical signal using two or more sampling windows contained within a time interval having a one-bit length to generate two or more bit estimate values;

(ii) apply a logical function to the two or more bit estimate values to generate a bit sequence corresponding to the optical signal;

(iii) integrate the electrical signal over a first sampling window to generate a first integration result;

(iv) compare the first integration result with a first decision threshold value to generate a first bit estimate value;

(v) integrate the electrical signal over a second sampling window to generate a second integration result; and

(vi) compare the second integration result with a second decision threshold value to generate a second bit estimate value, wherein:

the decoder comprises an "AND" gate adapted to apply an "AND" function to the first and second bit estimate values to generate a bit of the bit sequence.

21. (Canceled)

22. (Original) The system of claim 20, wherein the optical signal is an optical duobinary signal.

23. (Previously presented) The system of claim 20, wherein the optical receiver comprises:

a decision circuit coupled to the signal converter;

a clock recovery circuit coupled to the signal converter and adapted to generate a first clock signal based on the electrical signal;

a clock multiplier coupled between the clock recovery circuit and the decision circuit and adapted to multiply a frequency of the first clock signal to generate a second clock signal, wherein the decision circuit is adapted to sample the electrical signal at a sampling rate corresponding to the second clock signal to generate a bit stream carrying the first and second bit estimate values;

a de-multiplexer having an input port and a plurality of output ports, wherein:

the input port is coupled to the decision circuit;

a first output port is adapted to receive a signal corresponding to the first bit estimate value; and

a second output port is adapted to receive a signal corresponding to the second bit estimate value, wherein the "AND" gate is coupled to the first and second output ports.

24. (Previously presented) The system of claim 20, wherein the optical receiver comprises:

first and second decision circuits, each coupled to the signal converter;

a clock recovery circuit coupled between the signal converter and the first and second decision circuits and adapted to generate a clock signal based on the electrical signal, wherein:

each decision circuit is adapted to sample the electrical signal at a sampling rate corresponding to the clock signal;

the first decision circuit is adapted to generate the first bit estimate value;

the second decision circuit is adapted to generate the second bit estimate value; and

the first and second decision circuits sample the electrical signal with a relative time delay, wherein the "AND" gate is coupled to the first and second decision circuits.

25. (Previously presented) The system of claim 24, wherein:

each decision circuit is adapted to:

integrate the electrical signal over a respective sampling window to generate a respective integration result; and

compare the respective integration result with a respective decision threshold value to generate a bit estimate value; and

the first and second decision circuits use different decision threshold values.

EVIDENCE APPENDIX (37 CFR 41.37(c)(1)(ix))

None.

RELATED PROCEEDINGS APPENDIX (37 CFR 41.37(c)(1)(x))

None.

Respectfully submitted,

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/Yuri Gruzdkov/

Yuri Gruzdkov
Registration No. 50,762
Attorney for Appellant
(215) 557-8544 (phone)
(215) 557-8477 (fax)

Customer No. 46900
Mendelsohn, Drucker, & Associates, P.C.
1500 John F. Kennedy Blvd., Suite 405
Philadelphia, Pennsylvania 19102